



Global Standards for the Microelectronics Industry

Google Study:

Could those memory failures be caused by design flaws?

Barbara P. Aichinger
Vice President New Business Development
FuturePlus Systems Corporation
www.FuturePlus.com
Barb.Aichinger@FuturePlus.com

Server Memory Forum Shenzhen 2012

What was the Google Study?

- DRAM Errors in the Wild: A Large-Scale Field Study Schroeder, Pinheiro, Weber; SIGMETRICS/Performance '09 June
- This study tried to make sense of memory failures in Google's fleet of servers
 - Concluded that failures were orders of magnitude more prevalent than advertised
 - No specific conclusion could be reached as to the source of the errors
 - Noted that some failures followed the server versus the memory

Additional Conclusions

- 1.3% was the average Uncorrectable error rate across the fleet per year
 - Some platforms experienced 2-4% error rate per year
- Temperature had a small effect on error rate
- Newer Generation DIMMs did not show worse error rates as commonly feared (DDR1, DDR2 and FBDIMM)

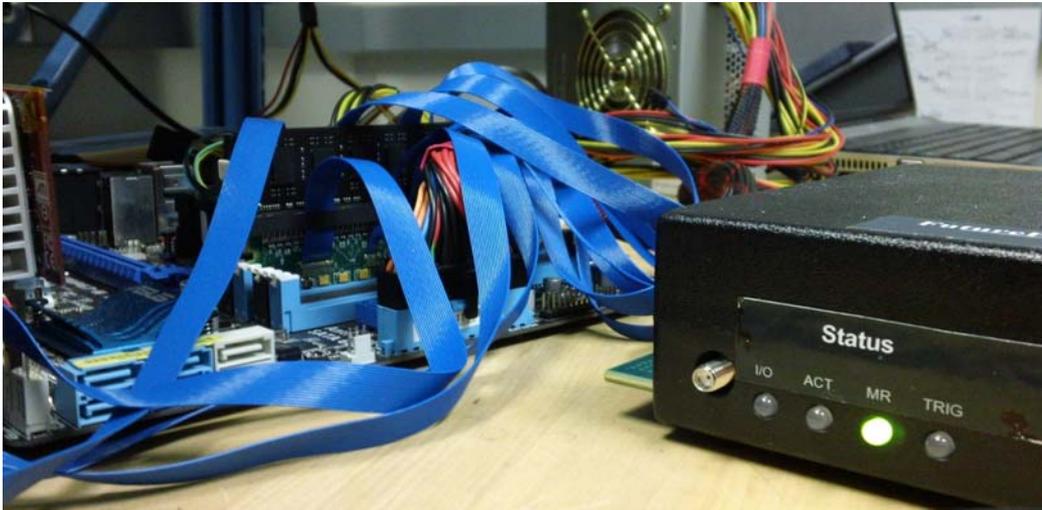
A Paradigm Shift for Memory Compliance Testing

- The Google Study did not have the advantage of the new tools that can automate Protocol Compliance Testing *In The Wild*
- Their conclusions could not find the source of the unexpectedly high error rate
- Improvement in error rates is critical to industries that rely upon large fleets of Servers

What is Protocol Compliance?

- Correct Timing between events on the DDR memory bus
- DDR3 Example:
 - Read operation followed by a Precharge
 - Write command followed too quickly by a Read command
 - Average Refresh rate

Our Study



- Commercially available motherboards
- FuturePlus Systems DDR3 Detective™
- DIMMs and a FuturePlus DIMM interposer



Examples of Protocol Compliance Failures

<p>Violation 1 MRS to MRS (tMRD) and MRS to other command (tMOD)</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 11 Any CS# asserted for more than 1 cycle or CS# to any CS#</p> <p>Main ■ Satellite ■ 0</p>	<p>Violation 24 Different rank WR to RD</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 36 PDE followed by non-NOP/DES</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>
<p>Violation 2 ACT To RD or WR (tRCD)</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 12 ACT to PRE</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 26 Different rank WR to WR</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 37 Power Down min time</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>
<p>Violation 3 PRE to ACT in the same bank or ZQCL/ZQCS/MRS or SRE (tRP)</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 13 ACT to PRE, PREA or ACT to AP</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 28 REF to REF over the last 128 intervals is greater than REF1</p> <p>R0 ■ R1 ■ R2 ■ 4571 R3 ■</p>	<p>Violation 38 Power Down max time</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>
<p>Violation 4 RD to PRE in the same bank (tRTP)</p> <p>R0 ■ R1 ■ R2 ■ 5334 R3 ■</p>	<p>Violation 14 Same rank RD To WR</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 29 ZQCS to Non-NOP/DES and ODT < ZQOper</p> <p>R0 ■ R1 ■ R2 ■ 1202 R3 ■</p>	<p>Violation 39 PDX Fast Exit</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>
<p>Violation 5 WR to WR Cmd in the same bank (tCCD)</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 15 WR to PRE or PREA</p> <p>R0 ■ R1 ■ R2 ■ 5334 R3 ■</p>	<p>Violation 30 WR w/AP to XXX</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	
<p>Violation 6 REF to an Non NOP/DES (tRFC)</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 16 Same rank WR to RD</p> <p>R0 ■ R1 ■ R2 ■ 5334 R3 ■</p>	<p>Violation 31 More than 4 ACTs in less than tFAW</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	
<p>Violation 7 SRX followed by non-NOP/DES (tXS)</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 17 Active bank check(s)</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	<p>Violation 32 RD/WR to CKE low or MRS violation</p> <p>R0 ■ R1 ■ R2 ■ 0 R3 ■</p>	

A READ to PRECHARGE Rank 0 Bank 5 separation fails by 1 clock

DDR3 Detective (On-Line) - [State Listing]

File Windows Help

Run Stop Setup Mode Registers Violations Performance Log File State Listing Eye Detector Setup Wizard

Columns T M1 7 Clks *Should be 8 clks*

State	TIME	Addr	BA	DDR3	PV	PC	CKE1
-16	4.2717ns	0358	6	WR Rank 1 Bank=6 Row=2B4E Column=358	0		1
-15	3.2038ns	0388	5	RD Rank 0 Bank=5 Row=2AF2 Column=388	0		1
-14	4.2717ns	0390	5	RD Rank 0 Bank=5 Row=2AF2 Column=390	0		1
-13	4.2717ns	03A0	5	RD Rank 0 Bank=5 Row=2AF2 Column=3A0	0		1
-12	4.2717ns	0398	5	RD Rank 0 Bank=5 Row=2AF2 Column=398	0		1
-11	4.2717ns	03A8	5	RD Rank 0 Bank=5 Row=2AF2 Column=3A8	0		1
-10	4.2717ns	03B0	5	RD Rank 0 Bank=5 Row=2AF2 Column=3B0	0		1
-9	4.2717ns	03C0	5	RD Rank 0 Bank=5 Row=2AF2 Column=3C0	0		1
-8	4.2717ns	03B8	5	RD Rank 0 Bank=5 Row=2AF2 Column=3B8	0		1
-7	4.2717ns	03C8	5	RD Rank 0 Bank=5 Row=2AF2 Column=3C8	0		1
-6	4.2717ns	03D0	5	RD Rank 0 Bank=5 Row=2AF2 Column=3D0	0		1
-5	4.2717ns	03E0	5	RD Rank 0 Bank=5 Row=2AF2 Column=3E0	0		1
-4	4.2717ns	03D8	5	RD Rank 0 Bank=5 Row=2AF2 Column=3D8	0		1
-3	4.2717ns	03E8	5	RD Rank 0 Bank=5 Row=2AF2 Column=3E8	0		1
-2	4.2717ns	03F0	5	RD Rank 0 Bank=5 Row=2AF2 Column=3F0	0		1
M1 -1	4.2717ns	03F8	5	RD Rank 0 Bank=5 Row=2AF2 Column=3F8	0		1
T 0	7.4755ns	0000	5	PRE Rank 0 Bank=5	1	V4	1
1	4.2717ns	02F0	3	WR Rank 0 Bank=3 Row=2AB8 Column=2F0	0		1
2	4.2717ns	0348	3	WR Rank 0 Bank=3 Row=2AB8 Column=348	0		1
3	1.0679ns	3F6E	5	ACT Rank 0 Bank=5 Addr=3F6E	0		1
4	3.2038ns	0218	3	WR Rank 0 Bank=3 Row=2AB8 Column=218	0		1
5	7.4755ns	03F8	6	WR Rank 1 Bank=6 Row=2B4E Column=3F8	0		1
6	4.2717ns	0320	6	WR Rank 1 Bank=6 Row=2B4E Column=320	0		1
7	4.2717ns	0330	6	WR Rank 1 Bank=6 Row=2B4E Column=330	0		1
8	4.2717ns	0175	5	RD Rank 0 Bank=5 Row=3F6E Column=175	0		1
9	4.2717ns	0370	5	RD Rank 0 Bank=5 Row=3F6E Column=370	0		1
10	11.7472ns	03A0	3	WR Rank 0 Bank=3 Row=2AB8 Column=3A0	0		1
11	4.2717ns	0308	3	WR Rank 0 Bank=3 Row=2AB8 Column=308	0		1
12	4.2717ns	0368	3	WR Rank 0 Bank=3 Row=2AB8 Column=368	0		1
13	4.2717ns	0238	3	WR Rank 0 Bank=3 Row=2AB8 Column=238	0		1
14	4.2717ns	0328	3	WR Rank 0 Bank=3 Row=2AB8 Column=328	0		1
15	4.2717ns	0380	3	WR Rank 0 Bank=3 Row=2AB8 Column=380	0		1

Ready

How critical is this failure?

- A Precharge closes a bank
- Read latency dictates when the data is to be returned
- Command telling the bank to close could be coincident with the data being returned from the bank

Write followed too quickly by a Read to the same RANK

DDR3 Detective (On-Line)

File Windows Help

Run Stop Setup Mode Registers Violations Performance Log File State Listing Eye Detector Setup Wizard

State Listing

Columns T MO 19 Clks *Should be 20 clks*

State	TIME	DDR3	BA	Addr	PV	PC
-20	1.0679ns	Deselect	1	0200	0	
MO -19	1.0679ns	WR Rank 0 Bank=1 Row=2BCA Column=22	1	0220	0	
-18	1.0679ns	Deselect	1	0220	0	
-17	1.0679ns	Deselect	1	0220	0	
-16	1.0679ns	Deselect	1	0220	0	
-15	1.0679ns	Deselect	1	0220	0	
-14	1.0679ns	Deselect	1	0220	0	
-13	1.0679ns	Deselect	1	0220	0	
-12	1.0679ns	WR Rank 1 Bank=7 Row=2BA4 Column=21	7	0210	0	
-11	1.0679ns	Deselect	7	0208	0	
-10	1.0679ns	Deselect	7	0208	0	
-9	1.0679ns	Deselect	7	0208	0	
-8	1.0679ns	WR Rank 1 Bank=7 Row=2BA4 Column=20	7	0208	0	
-7	1.0679ns	Deselect	7	0210	0	
-6	1.0679ns	Deselect	7	0210	0	
-5	1.0679ns	Deselect	7	0210	0	
-4	1.0679ns	WR Rank 1 Bank=7 Row=2BA4 Column=25	7	0250	0	
-3	1.0679ns	Deselect	7	0228	0	
-2	1.0679ns	Deselect	7	0228	0	
-1	1.0679ns	Deselect	7	0228	0	
T 0	1.0679ns	RD Rank 0 Bank=7 Row=2C00 Column=24	7	0240	1	V16
1	1.0679ns	Deselect	7	0240	0	
2	1.0679ns	Deselect	7	0240	0	
3	1.0679ns	Deselect	7	0240	0	
4	1.0679ns	RD Rank 0 Bank=7 Row=2C00 Column=23	7	0238	0	
5	1.0679ns	Deselect	7	0238	0	
6	1.0679ns	Deselect	7	0238	0	
7	1.0679ns	Deselect	7	0238	0	
8	1.0679ns	RD Rank 0 Bank=7 Row=2C00 Column=25	7	0250	0	
9	1.0679ns	Deselect	7	0250	0	

How critical is this failure?

- The parameters for the separation of the Write and the Read are based on the latencies
- The Data bus is shared and overlapping events can lead to data corruption

Data Corruption?

The image displays two screenshots from an Agilent Logic Analyzer and DDR3 Detective tool. The left screenshot shows a DDR3 Decoder COMMAND listing with two events highlighted: a write command at -208.1 ns and a read command at -176.1 ns. The right screenshot shows a DDR3 Detective listing with a table of events. Two red arrows point from the events in the right table to the corresponding events in the left table.

DDR3 Decoder COMMAND Listing (Left):

Sample Number	Time	DDR3 Decoder COMMAND	RE
-218.5		Data = E7BF9AA2 9564B263	
-218.6		Data = DBF3B18F FD98B5E8	
-218.7		Data = 789205EB 47F682C7	
-218.8		Data = F46B1F17 93A453DB	
-218.9		Data = 711A8D63 1ED7DEA7	
-218.10		Data = D0E13D9D 7BC614F7	
-218.11			
-217	-115.440 ns		
-208	-110.640 ns	Write CKE0 and CKE1 Enabled	
-208.1		Bank = 5 Rank 0	
-208.2		Address = 2BA3 01B8	
-208.3		Data = FB9B55E7 BFD5F7FB	
-208.4		Data = 2DAEC6B2 2719C028	
-208.5		Data = C0373C2E FF12956E	
-208.6		Data = 0CB066A9 9656DB67	
-208.7		Data = CD65B61C EB7F0505	
-208.8		Data = BB95D1EC D44EBB75	
-208.9		Data = 615A8C43 E5E8A1D0	
-208.10		Data = 026A6813 B644D973	
-208.11			
-207	-110.080 ns		
-176	-93.600 ns	Read CKE0 and CKE1 Enabled	
-176.1		Bank = 7 Rank 0	
-176.2		Col = 00F8	
-176.3		Data = FFFFFFFF FFFFFFFF	
-176.4		Data = 5945A55C BF26D55F	
-176.5		Data = 0591EEED C6CF8BB5	
-176.6		Data = 9DFAF783 DA8C1FF9	
-176.7		Data = 5E33232F 72531826	
-176.8		Data = B6D25BCB 113C7249	
-176.9		Data = 2712C6AE FE3E8D0D	

DDR3 Detective Listing (Right):

State	TIME	DDR3	PC
-18[966]	-19.1494ns[972]	Deselect	
-17[967]	-18.0856ns[973]	Deselect	
-16[968]	-17.0217ns[974]	WR #S0 Active Bank=5 Column=1B8	
-15[969]	-16.9578ns[975]	Deselect	
-14[970]	-14.8940ns[976]	Deselect	
-13[971]	-13.8302ns[977]	Deselect	
-12[972]	-12.7663ns[978]	Deselect	
-11[973]	-11.7024ns[979]	Deselect	
-10[974]	-10.6386ns[980]	Deselect	
-9[975]	-9.5747ns[981]	Deselect	
-8[976]	-8.5109ns[982]	Deselect	
-7[977]	-7.4470ns[983]	Deselect	
-6[978]	-6.3831ns[984]	Deselect	
-5[979]	-5.3193ns[985]	Deselect	
-4[980]	-4.2554ns[986]	Deselect	
-3[981]	-3.1916ns[987]	Deselect	
-2[982]	-2.1277ns[988]	Deselect	
-1[983]	-1.0639ns[989]	Deselect	
0[984]	0.0000ns[990]	RD #S0 Active Bank=7 Column=F8	V16
1[985]	1.0639ns[991]	Deselect	
2[986]	2.1277ns[992]	Deselect	
3[987]	3.1916ns[993]	Deselect	
4[988]	4.2554ns[994]	RD #S0 Active Bank=7 Column=100	
5[989]	5.3193ns[995]	Deselect	
6[990]	6.3831ns[996]	Deselect	
7[991]	7.4470ns[997]	Deselect	
8[992]	8.5109ns[998]	RD #S0 Active Bank=7 Column=F0	
9[993]	9.5747ns[999]	Deselect	
10[994]	10.6386ns[1000]	Deselect	
11[995]	11.7024ns[1001]	Deselect	
12[996]	12.7663ns[1002]	RD #S0 Active Bank=7 Column=E8	

A Write command followed too closely by a Precharge to the same bank

Should be 26 clks

State	Addr	TIME	BA	DDR3	PV	PC
	0098	1.0679ns	5	Deselect	0	
	0098	1.0679ns	5	Deselect	0	
	00A8	1.0679ns	5	WR Rank 0 Bank=5 Row=A0A Column=A8	0	
	00A8	1.0679ns	5	Deselect	0	
	00A8	1.0679ns	5	Deselect	0	
	00A8	1.0679ns	5	Deselect	0	
MO	0160	1.0679ns	5	WR Rank 0 Bank=5 Row=A0A Column=160	0	
	0160	1.0679ns	5	Deselect	0	
	0160	1.0679ns	5	Deselect	0	
	0170	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=170	0	
	00E8	1.0679ns	0	Deselect	0	
	00E8	1.0679ns	0	Deselect	0	
	00E8	1.0679ns	0	Deselect	0	
	0168	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=168	0	
	00F0	1.0679ns	0	Deselect	0	
	00F0	1.0679ns	0	Deselect	0	
	00F0	1.0679ns	0	Deselect	0	
	0178	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=178	0	
	00F8	1.0679ns	0	Deselect	0	
	00F8	1.0679ns	0	Deselect	0	
	00F8	1.0679ns	0	Deselect	0	
	0080	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=80	0	
	0100	1.0679ns	0	Deselect	0	
	0100	1.0679ns	0	Deselect	0	
	0100	1.0679ns	0	Deselect	0	
	0088	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=88	0	
	0110	1.0679ns	0	Deselect	0	
	0110	1.0679ns	0	Deselect	0	
	0110	1.0679ns	0	Deselect	0	
	0090	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=90	0	
T	0000	1.0679ns	5	PRE Rank 0 Bank=5	1	V15
1	0000	1.0679ns	5	Deselect	0	
2	0000	1.0679ns	5	Deselect	0	
3	0098	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=98	0	
4	0118	1.0679ns	0	Deselect	0	
5	0118	1.0679ns	0	Deselect	0	
6	0118	1.0679ns	0	Deselect	0	
7	00C0	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=C0	0	
8	0120	1.0679ns	0	Deselect	0	
9	3F6E	1.0679ns	5	ACT Rank 0 Bank=5 Addr=3F6E	0	
10	3F6E	1.0679ns	5	Deselect	0	
11	00D0	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=D0	0	
12	0128	1.0679ns	0	Deselect	0	
13	0128	1.0679ns	0	Deselect	0	
14	0128	1.0679ns	0	Deselect	0	
15	00C8	1.0679ns	0	RD Rank 1 Bank=0 Row=A27 Column=C8	0	
16	0130	1.0679ns	0	Deselect	0	

How critical is this failure?

- A Precharge command closes the bank
- The DRAM is not expecting the Precharge command and may depend on that time to complete the Write
- Thousands of times per minute over months and years of operation may lead to data corruption

Activate command too soon after a Calibration command

Should be 75 clks

State	TIME	DDR3	BA	Addr	PV	PC
-2	---	ZQCS Rank 0	0	0000	0	
-1	15.9290ms	ZQCS Rank 1	0	0000	0	
T 0	72.6191ns	ACT Rank 1 Bank=7 Addr=1A5F	7	1A5F	1	V29a
1	6.4076ns	ACT Rank 1 Bank=2 Addr=1A6D	2	1A6D	1	V29a
2	111.4840ms	ZQCS Rank 0	0	0000	0	
3	72.6191ns	ACT Rank 0 Bank=1 Addr=5E0	1	05E0	1	V29a
M0 4	15.9285ms	ZQCS Rank 1	0	0000	0	
M1 5	72.6191ns	ACT Rank 1 Bank=1 Addr=374	1	0374	1	V29a
6	111.4837ms	ZQCS Rank 0	0	0000	0	
7	71.5512ns	ACT Rank 0 Bank=1 Addr=1204	1	1204	1	V29a
8	6.4076ns	ACT Rank 0 Bank=5 Addr=11CC	5	11CC	1	V29a
9	15.9286ms	ZQCS Rank 1	0	0000	0	
10	72.6191ns	ACT Rank 1 Bank=2 Addr=155C	2	155C	1	V29a
11	111.4841ms	ZQCS Rank 0	0	0000	0	
12	72.6191ns	ACT Rank 0 Bank=0 Addr=29A5	0	29A5	1	V29a
13	6.4076ns	ACT Rank 0 Bank=7 Addr=296E	7	296E	1	V29a
14	15.9288ms	ZQCS Rank 1	0	0000	0	
15	72.6191ns	ACT Rank 1 Bank=0 Addr=2D19	0	2D19	1	V29a
16	6.4076ns	ACT Rank 1 Bank=6 Addr=2C60	6	2C60	1	V29a
17	111.4840ms	ZQCS Rank 0	0	0000	0	
18	71.5512ns	ACT Rank 0 Bank=2 Addr=3D95	2	3D95	1	V29a
19	6.4076ns	ACT Rank 0 Bank=7 Addr=3DCC	7	3DCC	1	V29a
20	15.9282ms	ZQCS Rank 1	0	0000	0	
21	72.6191ns	ACT Rank 1 Bank=3 Addr=3B44	3	3B44	1	V29a
22	6.4076ns	ACT Rank 1 Bank=7 Addr=3B3C	7	3B3C	1	V29a
23	111.4843ms	ZQCS Rank 0	0	0000	0	
24	72.6191ns	ACT Rank 0 Bank=3 Addr=2609	3	2609	1	V29a
25	6.4076ns	ACT Rank 0 Bank=2 Addr=2678	2	2678	1	V29a
26	15.9285ms	ZQCS Rank 1	0	0000	0	
27	111.4840ms	ZQCS Rank 0	0	0000	0	
28	71.5512ns	ACT Rank 0 Bank=6 Addr=E7C	6	0E7C	1	V29a
29	6.4076ns	ACT Rank 0 Bank=1 Addr=FB7	1	0FB7	1	V29a

How critical is this failure?

- Calibration commands – Purpose of calibrations is to account for voltage and temperature variations
- “No other activities should be performed on the DRAM channel by the controller for the duration of t_{ZQinit} , t_{ZQoper} , or t_{ZQCS} . The quiet time on the DRAM channel allows accurate calibrations of output driver and on-die termination values”
- If the DRAM does not expect the Activate Command it may be missed and the row not opened

A study of tREFI for the system under test

The screenshot shows a software interface with a menu bar (File, Windows, Help) and a toolbar (Run, Stop, Setup, Mode Registers, Violations, Performance, Log File, State Listing, Eye Detector, Setup Wizard). The main window displays a table of memory access events. The table has the following columns: State, TIME, DDR3, BA, Addr, PV, and PC. The data is as follows:

State	TIME	DDR3	BA	Addr	PV	PC
-26	3.8638us	REF Rank 0	0	0000	0	
-25	24.4940us	REF Rank 0	0	0000	0	
-24	25.2693us	REF Rank 0	0	0000	0	
-23	7.8439us	REF Rank 0	0	0000	0	
-22	3.1290us	REF Rank 0	0	0000	0	
-21	665.3184ns	REF Rank 0	0	0000	0	
-20	8.1675us	REF Rank 0	0	0000	0	
-19	417.5594ns	REF Rank 0	0	0000	0	
-18	2.5897us	REF Rank 0	0	0000	0	
-17	4.8804us	REF Rank 0	0	0000	0	
-16	363.0951ns	REF Rank 0	0	0000	0	
-15	12.0398us	REF Rank 0	0	0000	0	
-14	8.6822us	REF Rank 0	0	0000	0	
-13	4.4255us	REF Rank 0	0	0000	0	
-12	25.8257us	REF Rank 0	0	0000	0	
-11	8.0052us	REF Rank 0	0	0000	0	
-10	441.0538ns	REF Rank 0	0	0000	0	
-9	7.8397us	REF Rank 0	0	0000	0	
-8	517.9445ns	REF Rank 0	0	0000	0	
-7	2.2971us	REF Rank 0	0	0000	0	
-6	11.7408us	REF Rank 0	0	0000	0	
-5	7.5737us	REF Rank 0	0	0000	0	
-4	9.3070us	REF Rank 0	0	0000	0	
-3	2.7350us	REF Rank 0	0	0000	0	
-2	14.9403us	REF Rank 0	0	0000	0	
MO -1	484.8388ns	REF Rank 0	0	0000	0	
T 0	4.9210us	RD Rank 0 Bank=6 Row=22 Column=3E8	6	03E8	1	V28b
1	5.4827us	REF Rank 0	0	0000	0	
2	7.7756us	REF Rank 0	0	0000	0	
3	10.0374us	REF Rank 0	0	0000	0	
4	3.1162us	REF Rank 0	0	0000	0	
5	10.7818us	REF Rank 0	0	0000	0	
6	3.8787us	REF Rank 0	0	0000	0	
7	8.2177us	REF Rank 0	0	0000	0	
8	10.6600us	REF Rank 0	0	0000	0	

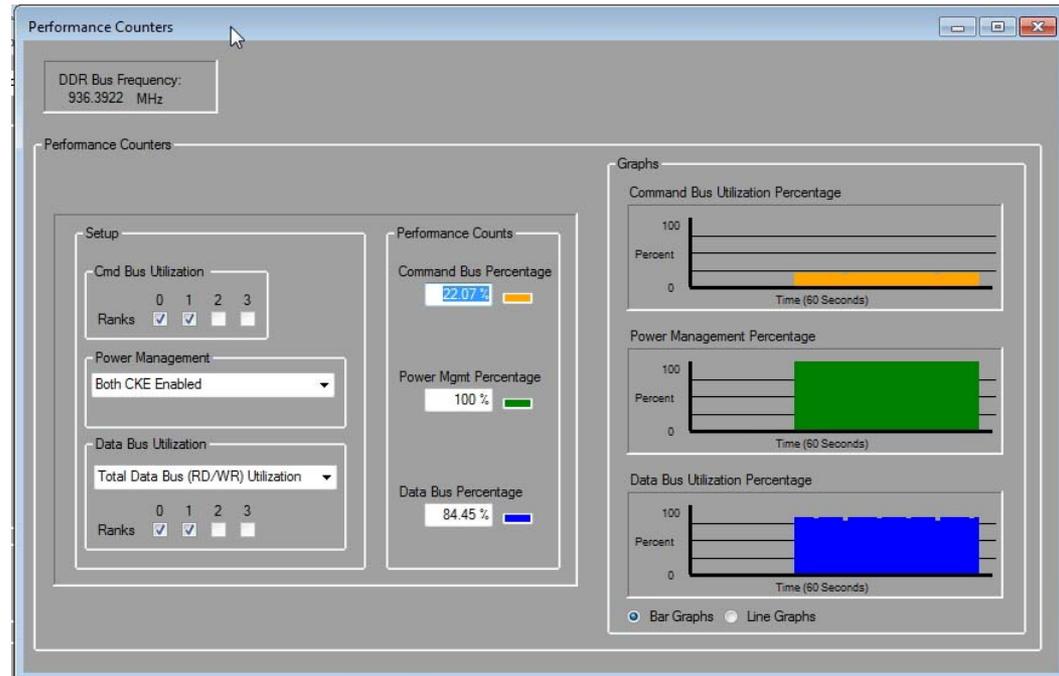
Refreshes

- Purpose is to maintain the integrity of the stored data
- Refresh too much: Waste power and bandwidth
- Refresh too little: Risk losing the data

Performance Metrics

Real time measurement gives insight

- Is power management as expected?
- Is Command bus and data bus utilization as expected?



Summary

- Real Time Protocol Compliance Analysis of this type is now possible
- Designers can now make systems more reliable and gain a better understanding of compliance and performance metrics
- As memory technology becomes more critical to our society this insight will help us write better specifications and provide better products

FuturePlus Systems Corporation

- Represented in China by CECEC

www.cecec.com.cn

- Represented in Shenzhen by HaoLun

www.haoluntech.com