



*Global Standards for the Microelectronics Industry*

# DDR Compliance Testing Its time has come!

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*Server Forum 2014*

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# DDR Compliance Testing

- If not then why now?
  - Continued growth and reliance on DDR memory
  - Critical applications increasing
  - Errors don't scale well
    - Large Data Centers replacing DIMMs every hour

# Several Publications point to error rate much larger than expected

- [DRAM Errors in the Wild: A Large-Scale Field Study](#) *Sigmatrics* 2009
- [Cosmic Rays Don't Strike Twice: Understanding the Nature of DRAM Errors and the Implications for System Design](#) by Andy Hwang, Ioan Stefanovici and Bianca Schroeder)
- [A Field Study of DRAM Errors](#) 2012 by Sridharan, Liberty, RAS Architecture AMD
- [Reliability, Serviceability and Availability: Intel XEON Processor E7 Family](#) April 2014
- [Characterizing Application Memory Error Vulnerability to Optimize Datacenter Cost via Heterogeneous-Reliability Memory](#) June 2014 Microsoft
- [Avoiding server downtime from hardware errors in system memory with HP Memory Quarantine](#) HP Technology Brief January 2012
- [Flipping bits in Memory Without Accessing Them: An Experimental Study of DRAM Disturbance Errors](#) by Yoongu Ki, et al Carnegie Mellon University and Intel Labs July 2014

# Open Compute Project



- Ready Certification
- Compliant Certification
  - Will point at other standards...if they exist
- Certification labs
  - University of Texas San Antonio
  - ITRI (Taiwan)
- You can Join! [www.OCP.com](http://www.OCP.com)

# National Institute of Standards and Technology

- Information Technology Laboratories
  - Cloud Computing Program

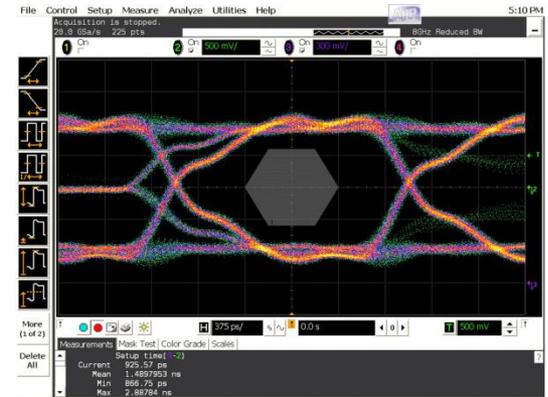
*“...It is **considered critical** that government and industry begin adoption of this technology in response to difficult economic constraints. ....Cloud computing is currently being used; however, security, interoperability, and portability are cited as major barriers to broader adoption....The long term goal is to provide thought leadership and guidance around the cloud computing paradigm to catalyze its use within industry and government. NIST aims to **shorten the adoption cycle**.... NIST aims to **foster cloud computing systems and practices** that support **interoperability, portability, and security requirements** that are appropriate and achievable for important usage scenarios.”*

# What would DDR4 Compliance Testing Look Like?

- DRAM specific
  - DIMM/SODIMM/LRDIMM
- Memory Controller specific
- The path between the two
- A Compliance Test Specification
  - T&M Vendors can produce MOI (Method of Implementation)
  - End users can then request this testing
    - Compliance Lab Testing

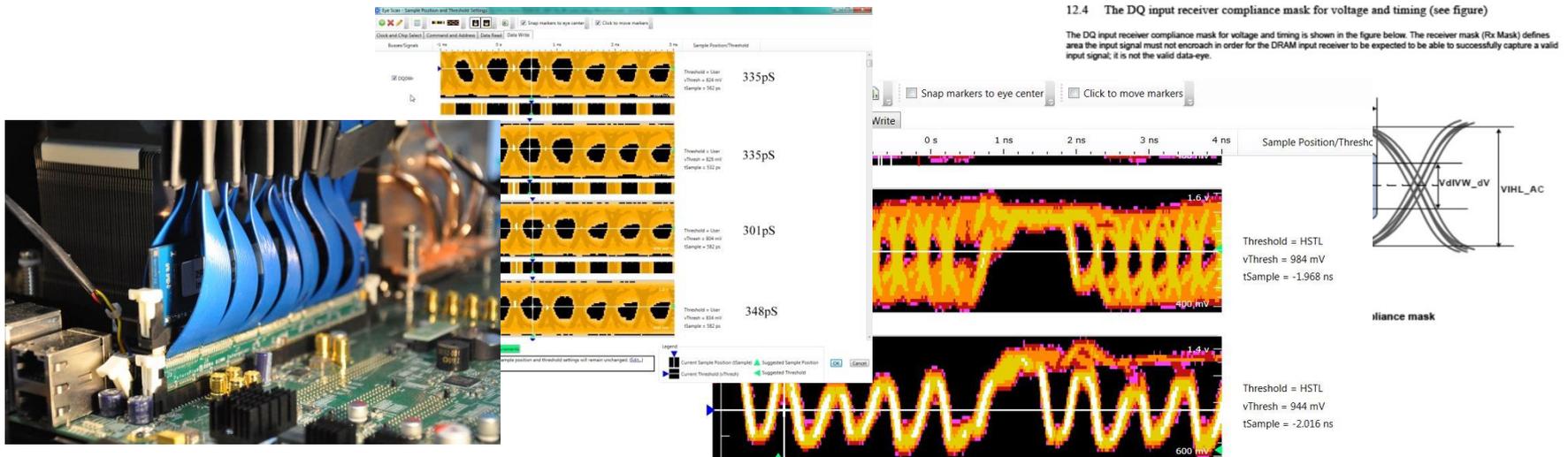
# DDR4 Compliance Testing

- Memory Controller Specific
  - RX/TX eye specification
    - Bit Error Rate
  - Protocol Violations
  - Timing Violations
  - Performance Specifications



# Memory Controller RX/TX

- Compliance Masks
- Measurement can be made with an interposer
  - Qualitative -> Quantitative

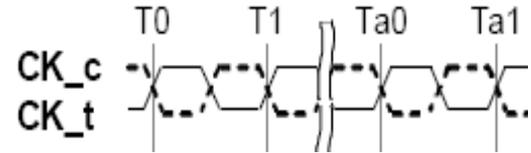


# Memory Controller *Protocol Violations*

- The DDR4 JEDEC spec contains rules on event ordering
  - Examples
    - Do not ACTIVATE a bank that is already open
    - Do not PRECHARGE a bank that is already closed
    - Do not RD/WR a non open page

# Memory Controller *Timing Violations*

- Clock edge boundary



- Things can not be too close together or too far apart

- Examples

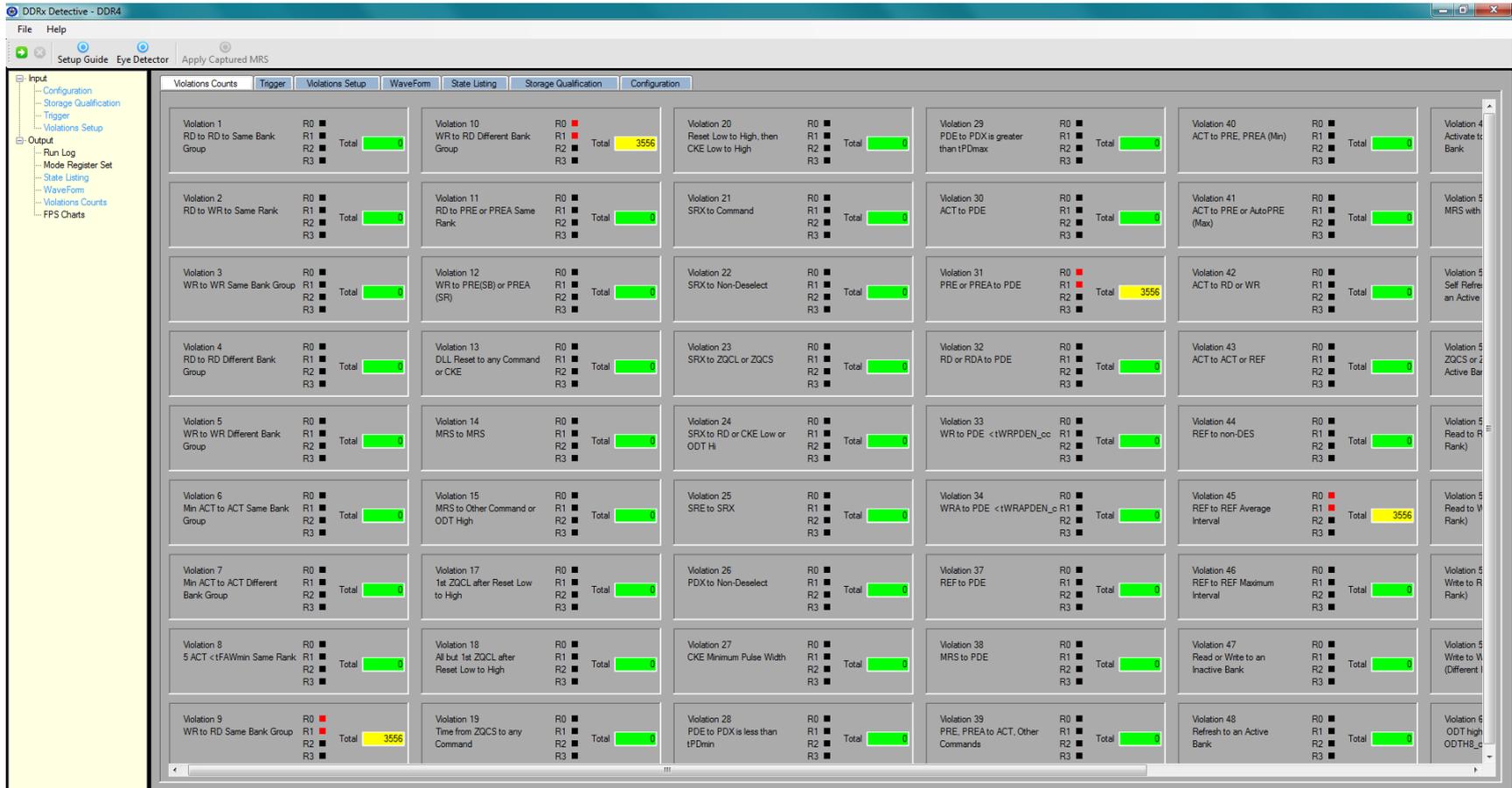
- tREFI Average refresh interval
- tRC ACT ot ACT or REF
- tMOD MRS to PDE
- tCCD\_L RD to RD to Same Bank Group

# 65 violations identified with over 1000+ simultaneous checks

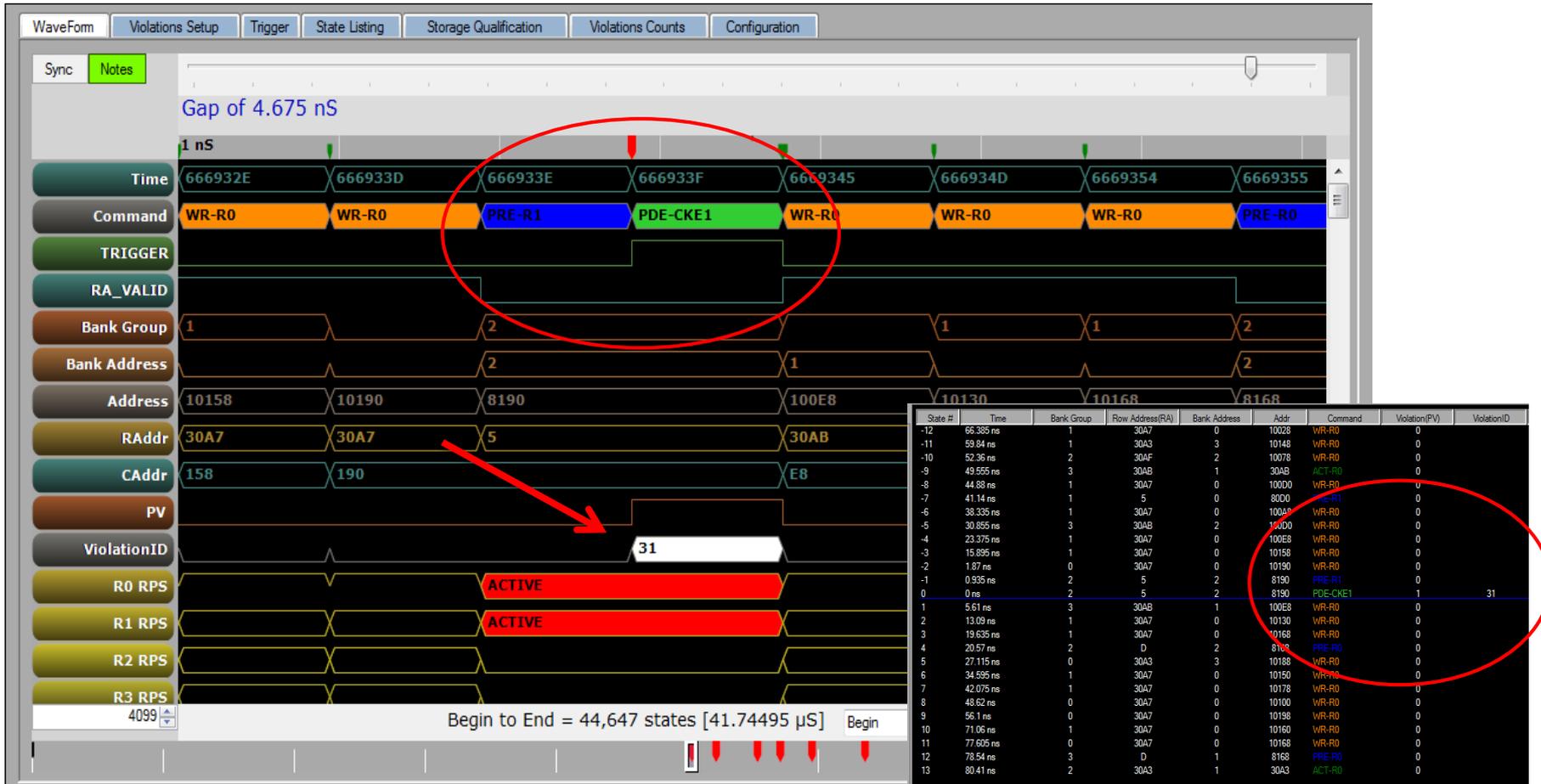
The screenshot displays a software interface for configuring and monitoring violations. It is divided into several sections:

- Violations Setup / Configuration:** The top navigation tabs.
- Select All / De-Select All:** Buttons to manage the selection of all checks.
- Violation List (Left Panel):** A list of 65 violations, each with a checkbox and a description. Most are checked. The list includes:
  - V1 - RD to RD to Same Bank Group
  - V2 - RD to WR to Same Rank
  - V3 - WR to WR Same Bank Group
  - V4 - RD to RD Different Bank Group
  - V5 - WR to WR Different Bank Group
  - V6 - Min ACT to ACT Same Bank Group
  - V7 - Min ACT to ACT Different Bank Group
  - V8 - 5 ACT < tFAWmin Same Rank
  - V9 - WR to RD Same Bank Group
  - V10 - WR to RD Different Bank Group
  - V11 - RD to PRE or PREA Same Rank
  - V12 - WR to PRE(SB) or PREA (SR)
  - V13 - DLL Reset to any Command or CKE
    - V13 ODT Enabled
  - V14 - MRS to MRS
  - V15 - MRS to Other Command or ODT High
    - V15 ODT Enabled
  - V16 - CA Bus and PAR\_IN have odd # of 1's
  - V17 - 1st ZQCL after Reset Low to High
    - V17 ODT Enabled
  - V18 - All but 1st ZQCL after Reset low to high
    - V18 ODT Enabled
  - V19 - Time from ZQCS to any Command
    - V19 ODT Enabled
  - V20 - Reset Low to High, then CKE Low to High
    - V20 ODT Enabled
  - V21 - SRX to Command
  - V22 - SRX to Non-Deselect
  - V23 - SRX to ZQCL or ZQCS
  - V24 - SRX to RD or CKE Low or ODT Hi
    - V24 ODT Enabled
  - V25 - SRE to SRX
  - V26 - PDX to Non-Deselect
  - V27 - CKE Minimum Pulse Width
  - V28 - PDE to PDX is less than tPDMIN
  - V29 - PDE to PDX is greater than tPDMAX
  - V30 - ACT to PDE
  - V31 - PRE or PREA to PDE
  - V32 - RD or RDA to PDE
  - V33 - WR to PDE < tWRPDCEN\_cc
  - V34 - WRA to PDE < tWRAPDCEN\_cc
  - V35 - WR to PDE < tWRPBC4EN\_cc
  - V36 - WR to PDE < tWRAPBC4EN\_cc
  - V37 - REF to PDE
  - V38 - MRS to PDE
  - V39 - PRE, PREA to ACT, Other Commands
  - V40 - ACT to PRE, PREA
  - V41 - ACT to PRE or AutoPRE
  - V42 - ACT to RD or WR
  - V43 - ACT to ACT or REF
  - V44 - REF to non-DES
  - V45 - REF to REF Average Interval
  - V46 - REF to REF Maximum Interval
  - V47 - Read or Write to an Inactive Bank
  - V48 - Refresh to an Active Bank
  - V49 - Activate to an Active Bank
  - V50 - MRS with an Active Bank
  - V51 - Self Refresh Entry with an Active Bank
  - V52 - ZQCS or ZQCL with an Active Bank
  - V53 - Read to Read (Different Rank)
  - V54 - Read to Read (Different DIMM)
  - V55 - Read to Write (Different Rank)
  - V56 - Read to Write (Different DIMM)
  - V57 - Write to Read (Different Rank)
  - V58 - Write to Read (Different DIMM)
  - V59 - Write to Write (Different Rank)
  - V60 - Write to Write (Different DIMM)
  - V61 - ODT high to Low Time < ODTH4\_cc
  - V62 - ODT high to Low Time < ODTH8\_cc
  - V63 - PDE or SRE Followed by non-DES
  - V64 - WRA, WRA to Command
  - V65 - RDA to Command
- Violation Details (Right Panel):** A scrollable list of 17 violations with their specific parameters and units:
  - V4 - RD to RD Different Bank Group: tCCD\_S 4 nClks[2-15]
  - V5 - WR to WR Different Bank Group: tCCD\_S 4 nClks[2-15]
  - V6 - Min ACT to ACT Same Bank Group: tRRD\_L 5 nClks[2-15]
  - V7 - Min ACT to ACT Different Bank Group: tRRD\_S 4 nClks[2-1023]
  - V8 - 5 ACT < tFAWmin Same Rank: tFAW 20 nClks[2-63]
  - V9 - WR to RD Same Bank Group: tWTR\_L 18 nClks[2-63]
  - V10 - WR to RD Different Bank Group: tWTR\_S 15 nClks[2-63]
  - V11 - RD to PRE or PREA Same Rank: tRTP 6 nClks[2-63]
  - V12 - WR to PRE(SB) or PREA (SR): tWR 25 nClks[2-127]
  - V13 - DLL Reset to any Command or CKE: tDLLK 597 nClks[2-1023]
  - V14 - MRS to MRS: tMRD 8 nClks[2-15]
  - V15 - MRS to Other Command or ODT High: tMOD 24 nClks[2-31]
  - V17 - 1st ZQCL after Reset Low to High: tZQint 1024 nClks[2-2047]

# Protocol and Timing Compliance 'in the wild'



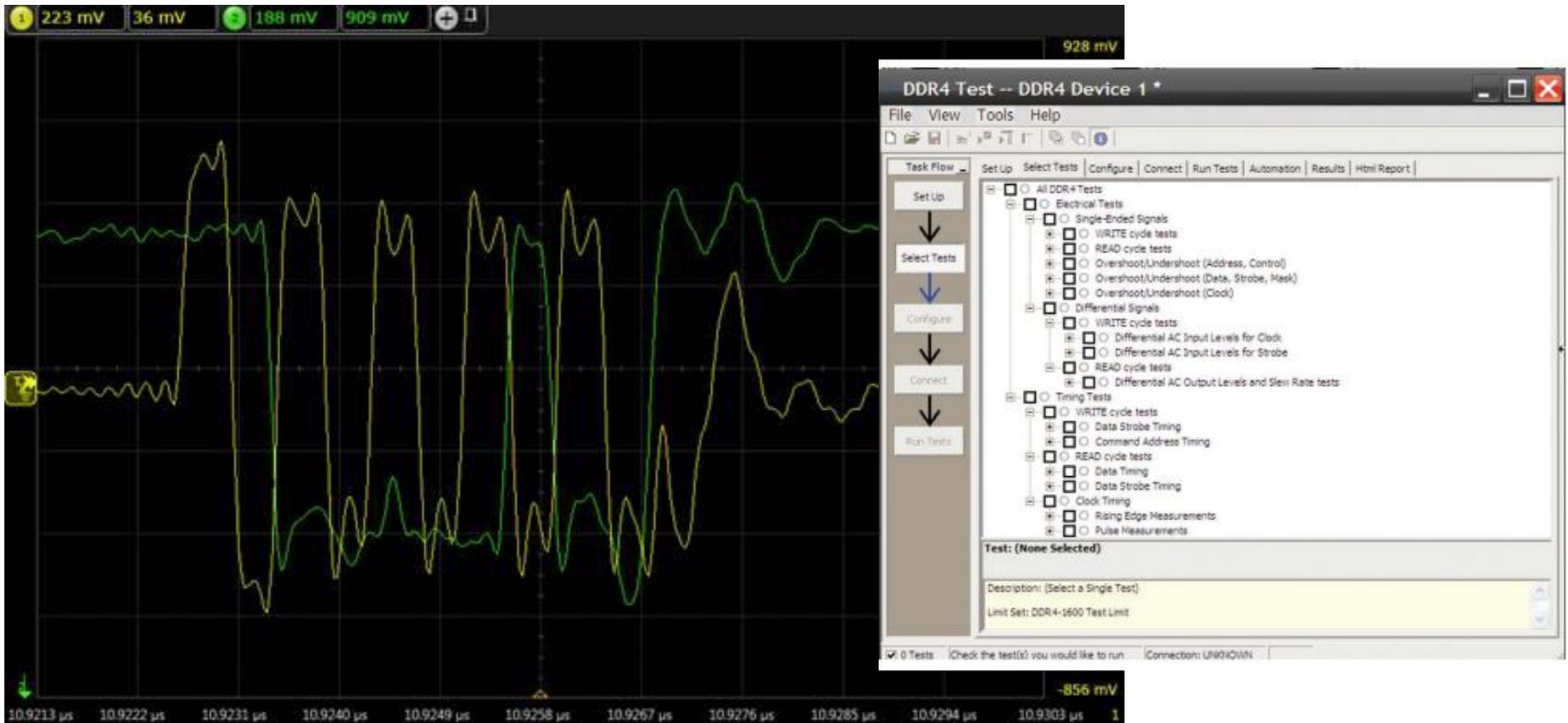
# JEDEC Specification Violation



# Memory Controller *Timing Violations*

- Timing that occurs between clock edges
  - Setup/Hold
  - Eye Mask
  - Jitter

# Several Scope Vendors have DDR4 Compliance Products



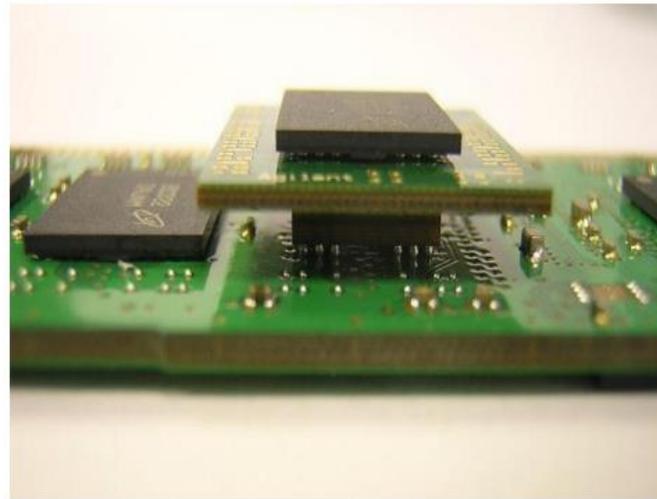
# Performance Metrics

- BER testing at particular transfer rates
  - 1E-16
- Which power management features are implemented
  - Is the clock stopped in Self Refresh?
  - Is Max Power Down implemented?

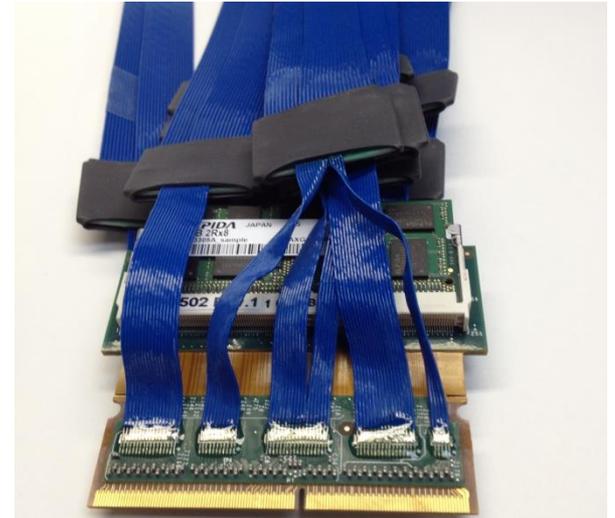
# DDR4 Compliance Testing

- DRAM Specific
  - DIMM/SODIMM/LRDIMM
  - RX/TX eye specification
    - Bit Error Rate
  - Data Integrity
    - Row Hammer (Excessive Activates)
  - Functional/Timing Verification
  - Performance Verification

# Making the Measurement



Photos Courtesy of Keysight Technologies

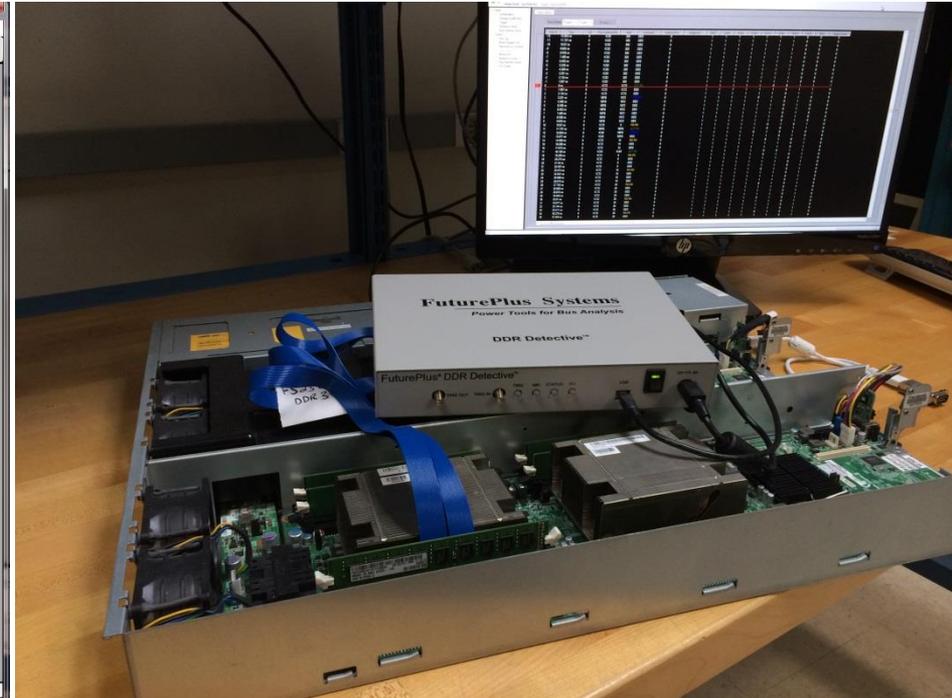
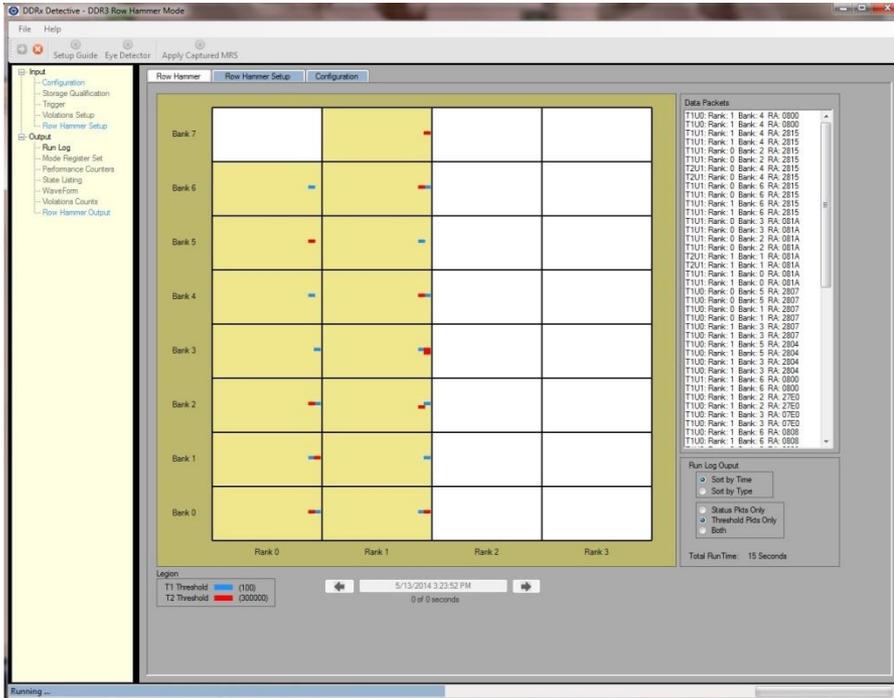


Photos Courtesy of FuturePlus Systems

# Row Hammer: Excessive Activates

- Yes its real.....easy to reproduce with software memory tests
- CMU study is the most recent technical paper on the topic
- Tools now look for it
- Data Centers are seeing it

# Row Hammer Detection



Row Hammer detection feature of the DDR Detective® lists the row address when the number of ACT commands exceeds a threshold within 64ms. Two programmable thresholds are available

Testing a Server for Row Hammer using the DDR Detective® with software from ThirdIO

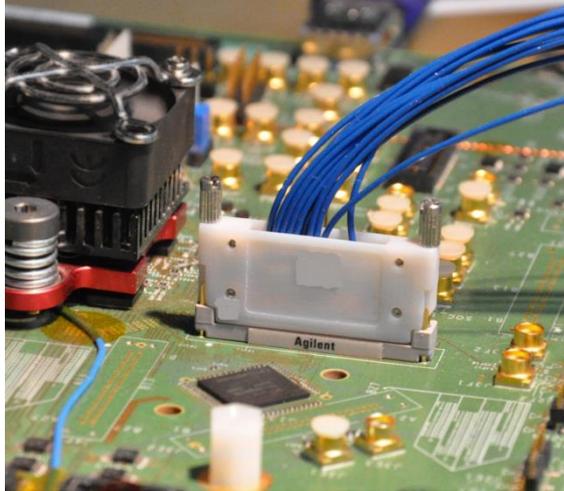
# The electrical path between the DRAM and the Memory Controller

- End to End Measurements to verify channel integrity
- Require Slot/Channel loading configurations based on speed/eye size
- Memory channel layout/board files with simulation results?
  - Similar to what is done today with raw cards

# What about the LP DDR specifications?

- Many of the tests are applicable and can be reused
- Probing becomes more difficult but can be accomplished
- Measuring Power Management features becomes more critical

# LPDDRx Compliance Test



# Advantages to having a Compliance Test Spec

- It is going to help our industry
  - End users are asking for this!
- Helps eliminate ambiguities in the specification
  - Ex:  $t_{REFI}$  = Average Refresh time...over how many cycles?
- Makes high quality validation easier and less costly

# My Contact Information

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